Claim Amendments

Please amend the claims as follows:

1. (Previously Presented) An I/O cell, comprising:

a bidirectional signal pad configured for transferring a first signal to a device coupled thereto and for receiving a second signal from the device;

a duty cycle controller coupled to the signal pad and configured for balancing a duty cycle of the first signal with respect to a clock signal; and

a dynamic switchable termination coupled to the signal pad and configured for providing a termination impedance when the I/O cell is receiving the second data signal.

2. (Original) The I/O cell of claim 1, wherein the duty cycle controller comprises a logic circuit configured for gating the first signal using the clock signal.

3. (Original) The I/O cell of claim 1, further comprising a controller configured for determining when the second signal is to be received from the signal pad and when the first signal is to be transferred to the signal pad.

4. (Original) The I/O cell of claim 3, wherein the dynamic switchable termination comprises a logic gate configured for receiving an enable signal from the controller when the second signal is to be received, wherein the logic gate enables the termination impedance based on the enable signal.

5. (Original) The I/O cell of claim 1, wherein the dynamic switchable termination comprises a process, voltage and temperature compensated resistor configured for providing the termination impedance.

6. (Original) The I/O cell of claim 1, wherein the duty cycle controller comprises a first flip-flop and a second flip-flop for gating the first signal with respect to the clock signal.

7. (Original) The I/O cell of claim 6, further comprising an output stage coupled between the duty cycle controller and the bidirectional signal pad and configured for providing the first signal to the bidirectional signal pad, wherein the output stage comprises a first transistor having a gate coupled to the first flip-flop and a second transistor having a gate coupled to the second flip-flop.

8. (Original) The I/O cell of claim 7, wherein the first transistor and the second transistor are process, voltage and temperature compensated transistors.

9. (Previously Presented) An I/O device, comprising:

an output signal pad configured for transferring a data signal to another device coupled thereto;

an output driver comprising a first transistor and a second transistor for providing the data signal to the output signal pad; and

a duty cycle controller comprising a first logic circuit coupled to a gate of the first transistor and a second logic circuit coupled to a gate of the second transistor, wherein the duty cycle controller is configured for balancing a duty cycle of the data signal with respect to a clock signal, and wherein the first logic circuit and the second logic circuit are adapted for gating the data signal to the output driver using the clock signal and the first logic circuit comprises a flip-flop.

10. (Cancelled)

11. (Cancelled)

12. (Previously Presented) The I/O device of claim 9, further comprising a controller for determining when the data signal is to be transferred to the signal pad.

13. (Original) The I/O device of claim 9, wherein the first and the second transistors are process, voltage and temperature compensated transistors.

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Previously Presented) A method for transceiving data, comprising:

transferring a first data signal to an externally coupled device comprising

balancing a duty cycle of a first data signal of the data with respect to a clock signal; and

receiving a second data signal of the data from the externally coupled device responsive to transferring and comprising

dynamically applying a termination impedance to the second data signal.

18. (Original) The method of claim 17, wherein balancing comprises gating the first data signal with a logic gate.

19. (Original) The method of claim 18, further comprising:

receiving the first data signal from the logic gate; and

outputting the first data signal with a process, voltage and temperature compensated transistor.

20. (Original) The method of claim 17, wherein dynamically applying comprises receiving a control signal to dynamically apply a process, voltage and temperature compensated resistor.